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DESIGN AND IMPLEMENTATION OF MULTILEVEL INVERTER TOPOLOGY WITH REDUCED SWITCHING COMPONENTS

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Abstract

Multilevel inverters play a vital role in renewable energy applications. In this paper we designed a new MLI topology for various renewable energy sources application with fewer switches using the multiple pulse width modulation technique. H-Bridge MLI topology is designed and implemented in an asymmetrical configuration. The equal amplitude of DC sources is symmetric, and unequal amplitude DC sources are used asymmetrically. On operating the MLI in an asymmetric design with four voltage sources, eight switches and 15-level output is produced, while in symmetric mode 9-level output is produced. The low-frequency modulation scheme is applied with a designed switching pattern where the switching period is pre-determined. The proposed topology is designed with reduced switches, minimal total harmonic distortion (THD) and the results are compared with conventional multilevel inverter topologies. The proposed MLI topology performance is validated and verified with number of switches and voltage levels and mainly LSR & CLF. Fifteen-level MLI operation is also simulated using MATLAB platform for experimental validation. The results produced by proposed topology are found to be encouraging and superior than any other conventional topology.

Key words: multilevel inverter, pulse width modulation, level number per switch ratio, component per level factor, total harmonic distortion

Introduction. Conventional energy sources lead to global warming due to CO_2 emissions. Renewable energy sources (RES) play a significant role in meeting

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the demand. The depletion of fossil fuels paved the way for the emergence of RES. Solar energy, and wind energy are the primary sources of renewable energy [1]. The reliability of power generation will increase with the integration of RES into the power grid. The major problem faced in Solar PV is maintaining the maximum power in all situations, which requires an appropriate converter topology to improve the output from the Solar PV. The various parameters that impact the selection of converter topologies have cost, the number of switches, efficiency and soft switching commutation.

The multilevel inverter (MLI) topology is mainly implemented to eradicate the problems concerning THD, electromagnetic interference and dv/dt stress on switches [2]. The need for MLI is increasing daily as many appliances depend on it. Thus, it is clear that MLI is beneficial for improving the harmonic profile and reducing the number of components, followed by cost reduction of the system [3]. The main concept is varying the voltage levels continuously at various magnitudes to get an effective and smoother waveform. The multilevel topology has several modulation techniques; one widely used method is pulse width modulation which helps to make the output more proper and adequate [4]. The motivation to utilize a multilevel inverter is to stabilize the nature of DC to AC conversion, which will alleviate the high losses and switching frequency seen in three-level inverters.

In this paper, the author designed a novel topology of MLI in two different ways: a system with 10 switches and three distinct voltage sources for 15 level of output and another topology comprising 12 switches for 25 level of output. The above two topologies are compared with different modulation index and the voltage stress across the switches are reduced. The researcher increased output levels to reduce switching loss and voltage stress [5,6]. The phase disposition sine PWM technique is implemented to modify the t-type multilevel inverter. Here they developed MLI through MATLAB software and executed the output through Hardware with the help of OPAL-RT. The researcher implemented modified dc link with an inverter with a carrier-based PWM technique [6]. The 7 levels of the output voltage is generated when the six switches are controlled. In this paper, topology is designed with one architecture for voltage of medium-level applications based on single-double source unit in symmetric and asymmetric ways. Under typical circumstances, the output can reach a maximum of 13 levels, though the proposed architecture includes two different kinds of hybrid topologies. In that, hybrid topology 1 produces 27 levels of output and hybrid topology 2 attains 21 levels [7–15].

Proposed topology. Figure 1(a) represents the block diagram of the proposed topology of MLI. The converter's input comes from renewable resources, such as solar PV, wind energy, or any DC source. The varying output collected from renewable energy sources is converted into boosted DC using the converter and fed to the MLI topology.

Asymmetric concept executed in MLI proposed topology. Figure 1(b) shows the proposed multilevel inverter topology with 8 switches. The topology is operated with four different voltages, namely V_1 = 12 V, V_2 = 24 V, V_3 = 48 V, V_4 = 48 V. Seven positive levels, 7 negative levels and one zero level have been obtained from the different modes of operation. Figure 2 shows the proposed topology of MLI with four different amplitudes of DC sources operating in asymmetrical mode. The new proposed MLI topology includes eight power semiconductor switches. It consists of six uni-directional switches (S_2, S_4, S_5, S_6, S_7, S_8) and two bidirectional switches (S_1, S_3).

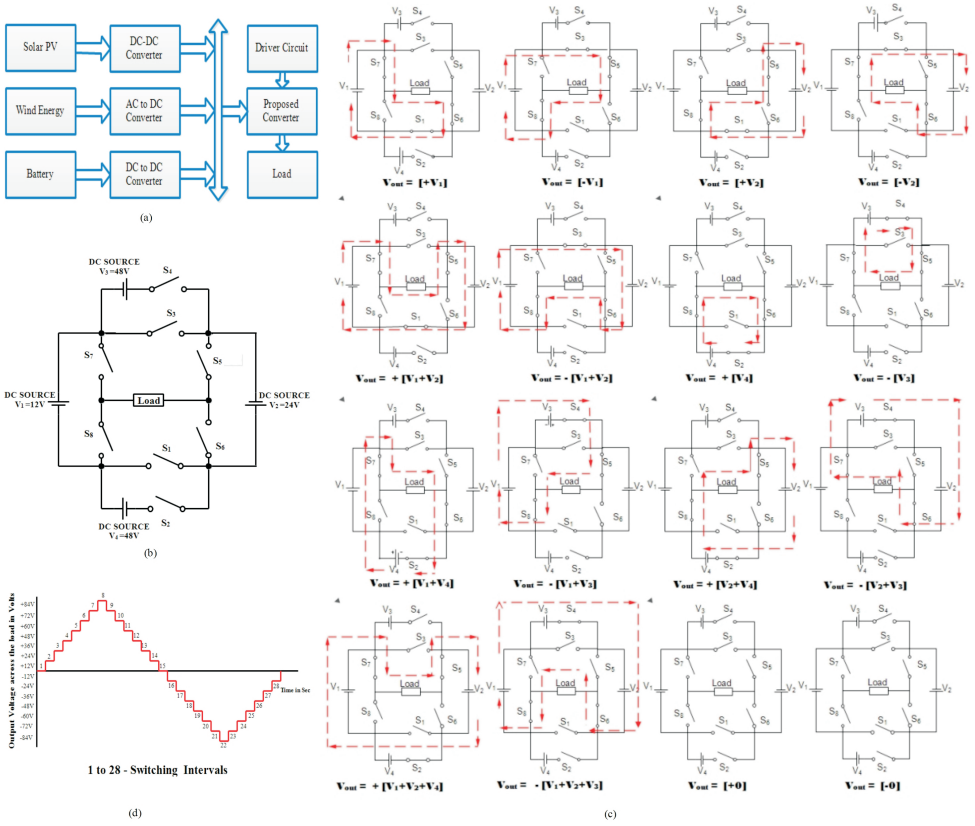


Fig. 1. a) Block Diagram of Proposed Topology; b) Proposed Topology; c) Modes of operation; d) Switching pattern design

Modes of operation. Figure 1(c) shows the different modes of operation, and Table 1 shows the power flow sequence across the load. Added voltages are monitored across the load to determine output voltage levels. Table 1 lists several combinations of switching states for the suggested voltages.

Parameters of the proposed MLI design. The circuit parameters of proposed topology:

Table 1

Proposed topology triggering sequence of switches

Interval	Power flow sequence							Output		Interval	Power flow sequence							Output
1	All switches open							0 V		15	All switches open							0 V
2	V_1	S_7	L	S_6	S_1	–	–	+12 V		16	V_1	S_3	S_5	L	S_8	–	–	−12 V
3	V_2	S_1	S_8	L	S_5	–	–	+24 V		17	V_2	S_6	L	S_7	S_3	–	–	−24 V
4	V_1	S_7	L	S_5	V_2	S_1	–	+36 V		18	V_2	S_6	L	S_8	V_1	S_3	–	−36 V
5	V_4	S_8	L	S_6	S_2	–	–	+48 V		19	V_3	S_4	S_5	L	S_7	–	–	−48 V
6	V_4	V_1	S_7	L	S_6	S_2	–	+60 V		20	V_1	V_3	S_4	S_5	L	S_8	–	−60 V
7	V_2	S_2	V_4	S_8	L	S_5	–	+72 V		21	V_3	S_4	V_2	S_6	L	S_7	–	−72 V
8	V_2	S_2	V_4	V_1	S_7	L	S_5	+84 V		22	V_1	V_3	S_4	V_2	S_6	L	S_8	−84 V
9	V_2	S_2	V_4	S_8	L	S_5	–	+72 V		23	V_3	S_4	V_2	S_6	L	S_7	–	−72 V
10	V_4	V_1	S_7	L	S_6	S_2	–	+60 V		24	V_1	V_3	S_4	S_5	L	S_8	–	−60 V
11	V_4	S_8	L	S_6	S_2	–	–	+48 V		25	V_3	S_4	S_5	L	S_7	–	–	−48 V
12	V_1	S_7	L	S_5	V_2	S_1	–	+36 V		26	V_2	S_6	L	S_8	V_1	S_3	–	−36 V
13	V_2	S_1	S_8	L	S_5	–	–	+24 V		27	V_2	S_6	L	S_7	S_3	–	–	−24 V
14	V_1	S_7	L	S_6	S_1	–	–	+12 V		28	V_1	S_3	S_5	L	S_8	–	–	−12 V

The number of switches are estimated as

$$J_{switch} = 6P \ + \ 2, \tag{1}$$

where P is the number of basic unit, then the number of switches is

$$J_{switch} = [6 \times 1] + 2 = 8 \ \text{ by taking } \ P = 1(15 \ - \ \text{level of output}).$$

The number of sources is calculated as

$$R_{source} = 4P. \tag{2}$$

Then the number of sources is

$$R_{source} = [4 \times 1] = 4 \text{ by taking } P = 1.$$

The number of levels is found by

$$D_{level} = (2 \times J_{switch}) - 1. \tag{3}$$

Then the number of levels is

$$D_{level} = [2 \times 8] - 1 = 15 \text{ by taking } J_{switch} = 8.$$

The output voltage is determined as

$$\mathrm{V_o} = \mathrm{V_1} + \mathrm{V_2} + \mathrm{V_3} + \mathrm{V_4}, \tag{4}$$

where $\mathrm{V_1} = 12$ V, $\mathrm{V_2} = 24$ V, $\mathrm{V_3} = 48$ V, $\mathrm{V_4} = 48$ V.

Results and discussion. This chapter discusses the output voltage, voltage across the load, FFT analysis, comparison of the number of switches used, and the number of voltage levels in symmetrical and asymmetrical configurations.

Simulation result of voltage across the load. Figure 2(a) shows how MATLab Simulink has obtained the fifteen levels of output. It represents the 15 positive and negative output voltage levels such as 12 V, 24 V, 36 V, 48 V, 60 V, 72 V, and 84 V.

Figure 2(b) shows the comparison of the number of switches used. The proposed topology has proved that the number of switches is smaller than the existing topology. Figure 2(c) shows the comparison of number of levels obtained in a symmetrical configuration. The proposed topology has proved that the number levels is equal to existing topology. Figure 2(d) shows the comparison of number levels obtained in asymmetrical configuration. The proposed topology represents 15 output levels compared with the existing topology (Fig. 2(g)).

Experimental setup. Figure 2(e) shows the experimental setup of the proposed MLI topology. The proposed prototype model clearly shows the setup

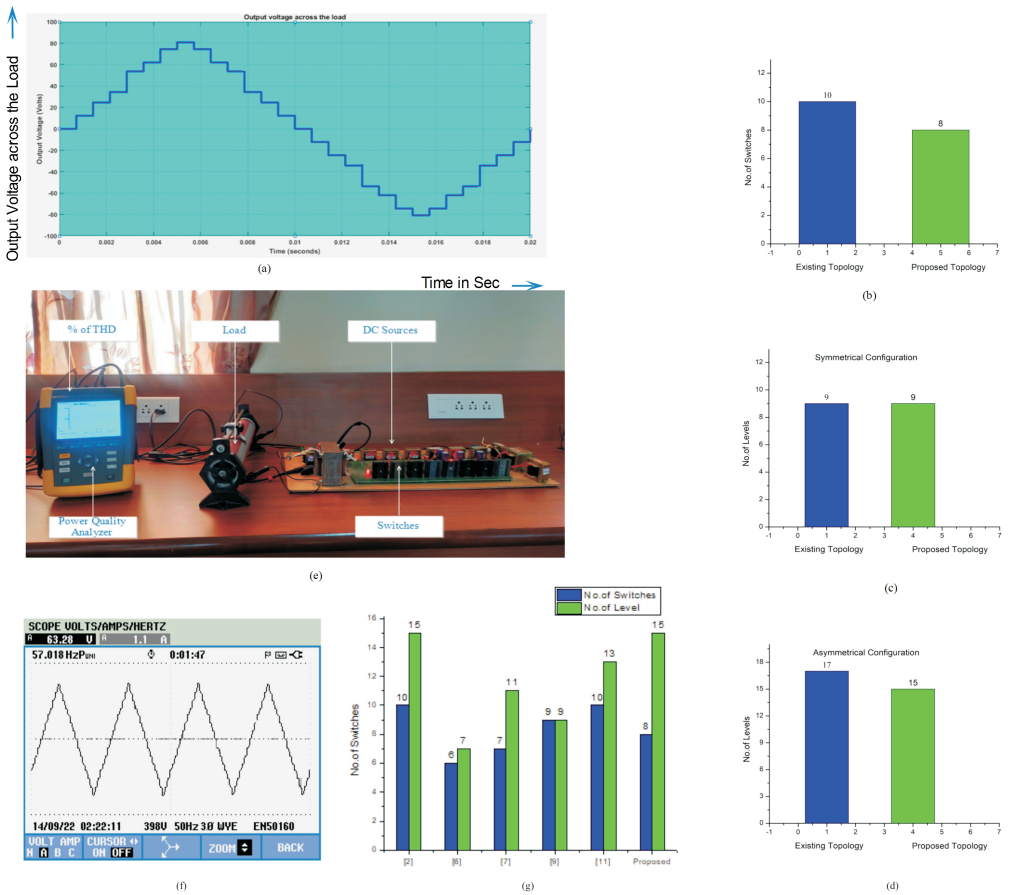


Fig. 2. a) Simulation result of voltage across the load; b) Comparison of number of switches; c) Comparison of number of levels in symmetrical configuration; d) Comparison of number of levels in asymmetrical configuration; e) Experimental setup for fifteen level MLI; f) Output voltage; g) Comparison of existing and proposed topology

comprising 8 MOSFET switches, four regulated voltage supplies, step-down transformers, optocouplers and LEDs. The output waveform generated through this setup is verified and displayed using an advanced digital storage oscilloscope. The prototype is operated with four different voltages namely $V_1 = 12$ V, $V_2 = 24$ V, $V_3 = 48$ V, $V_4 = 48$ V to provide maximum output voltage of 63 V. The complete cycle of the waveform is obtained with 15 levels of voltage composed of 7 levels in each positive and negative level and one zero level. Hardware specification and rating for various operating parameters are input voltages – 12 V, 24 V, 48 V, MOSFET with Fast recovery diodes – IRFP 460 with BYF229, output voltage – 63 V, output current – 1.1 amp, load resistor – 100 Ω.

Figure 2(e) represents the 15 levels of output voltage obtained from the experimental setup. From the output waveform, it is clear that the fifteen-level

output voltage is turned and obtained by the digital storage oscilloscope. Eight MOSFET switches with heat sinks are employed in the hardware prototype. The pulse generator generated the pulse signals and fed them to turn on the switches through the control terminal. Here, the controller and MOSFET switches are properly isolated using an optocoupler. The MLI receives its input supply via a transformer. Transformers initially reduce 230 V AC electricity to 12 V AC, and rectifiers convert AC to DC. For the input supply of 12 V, the voltage regulator LM7812 is utilised, and the voltage regulator LM7805 is used to generate 5 V for Arduino operation. The Load Rheostat is connected to MLI's output.

Figure 2(f) shows the output waveform collected from Power Quality Analyser while connecting across the load. The output waveform comprises of 15 levels, which include both positive and negative cycle in equal numbers. Initially, the system suffers from severe harmonics; while increasing the stages, the amount of harmonics gradually decreases. The system is recorded with an output of 63.28 V and 1.1 amp current across the load. A power quality analyser is used to measure the total harmonics present in the output. Figure 2(f) shows the total harmonic distortions present in the 15 level MLI when the load is resistive. It clearly shows that the amount of THD measured in the power quality analyser is 13.4%. Further it can suppress the harmonic suppression with help of filters [13].

From Table 2 it is clear that the various multilevel inverters consisting of H bridge topologies have been discussed and compared with the proposed topology regarding the number of sources, diodes, switches, levels, total number of components, LSR and CLF, correspondingly. The increased number of voltage levels (15 levels) when compared with existing topologies, namely MLI with 9 switches and 15 levels [16], MLI with 6 switches and 7 levels [17], MLI with 7 switches and 11 levels [18], MLI with 9 switches and 9 levels [19], MLI with 10 switches and 13 levels [20]. Compared with the topology mentioned above, the proposed topology is effective in operation, which comprises of the reduced num-

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Comparison of existing topologies with proposed topology

Reference paper	No. of sources	No. of diodes	No. of switches	Total No. of components	No. of levels	CLF	LSR
[16]	3	–	9	12	15	**0.80**	1.67
[17]	2	6	6	14	7	2.00	1.17
[18]	3	–	7	10	11	0.91	1.57
[19]	4	3	9	16	9	1.78	1.00
[20]	5	–	10	15	13	1.15	1.30
Proposed	4	–	8	12	15	**0.80**	**1.87**

ber of switches, namely of 8 switches and increased levels of operation up to 15 levels. The proposed topology is better than conventional topology by higher LSR of 1.87, lower CLF of 0.80. Figure 2(g) compares the LSR and CLF for different topologies. The ratio of number of levels generated and number of switches is the Level number per Switch Ratio (LSR) and also the number of levels generated by each switch. Higher value of LSR denotes the better topology as compared with other topologies. Component Per Level Factor (CLF) is the ratio of total number of components used and number of levels. Lesser value of CLF will lead to better topology as compared with other topologies.

Losses and efficiency. Inverter Power Loss in MOSFET the loss due to conduction:

$$P_{cl,T(t)} = [V_{MOSFET} + (R_{MOSFET} \times I_{rms})] \times I_{rms} \times P_{lsw}. \tag{5}$$

Loss due to switching:

$$T_{on} = V_{rms} \times I_{rms}(t_{on\ delay} \times t_{on\ rise}) \times P_{lsw} \tag{6}$$

$$T_{off} = V_{rms} \times I_{rms}\,(t_{off\ delay} \times t_{on\ fall}) \times P_{lsw}. \tag{7}$$

Energy losses are estimated as follows:

$$P_{sl} = T_{on} + T_{off}. \tag{8}$$

The total power losses ($P_{total\ loss}$) are estimated as follows:

$$P_{total\ loss} = P_{cl} + P_{sl}. \tag{9}$$

Inverter efficiency. Here P_{out} is the Output power; P_{in} is the Input power. The output power can be estimated as follows:

$$P_{out} = V_{rms} \times I_{rms}. \tag{10}$$

MLI efficiency (η) is given as

$$\eta = \frac{P_{out}}{P_{in}} = \left[\frac{P_{out}}{P_{out} + P_{total\ loss}}\right] \times 100 \tag{11}$$

$$\eta = \left[\frac{59.41}{59.41 + 4}\right] \times 100 = 0.9369 \times 100 = 93.69\%.$$

The simulation output power, P_o = 59.41 W is obtained (V_{rms} = 59.41 V & I_{rms} = 1 A). P_{in} represents the inverter's input power, and P_{out} represents the output power. The total losses and efficiency are computed with the help of MATLAB simulation. The input power fed into the inverter is 63.41 W, the R_{ds}

(on) is 0.85 ohm, and VDS (on) is 0.8 V where assigned for the switches. The load output power is obtained as 59.41 W, and efficiency is achieved as 93.69%. The results of input power, output power, efficiency, and total losses are obtained.

Conclusion. This paper proposes a new topology for a MLI with a lower switch count of eight and executed in symmetrical and asymmetrical configuration possibilities with four voltage sources. When the system configuration comprises an equal magnitude of voltage i.e. in a symmetrical configuration, the multilevel inverter generates nine-level output voltage. The system operates in unequal voltage magnitude during the asymmetric configuration and generates fifteen-level output voltage. While extending the MLI topology to further extension by cascading configuration produces twenty-nine level output voltage, respectively. The fifteen-level MLI has a lower THD of about 13.4% without connecting the filter in experimental and improved voltage conversion ratio results in more efficiency. The proposed MLI topology results are compared with the recently developed topology in terms of the number of switches, number of levels, and mainly LSR & CLF. The proposed topology is found to be superior when compared with conventional topology.

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