

MODELLING OF DIFFERENT ON-CHIP INDUCTORS FOR RADIO FREQUENCY INTEGRATED CIRCUITS

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Abstract

This paper presents a typical frequency-dependent modelling of different on-chip inductors for RFICs design problems. Modern RF circuits often feature on-chip inductors required by modern circuit design. A comparison of different inductor geometries includes a planar spiral inductor and novel multilayer inductors are analyzed. An electromagnetic model with fewer assumptions than empirical equations and higher efficiency than full-field solvers would be welcome. So would facile comparisons of different inductor structures. This paper describes recent work on the electromagnetic modelling of on-chip inductor structures, applied to the comparison of inductor geometries, including the traditional spiral inductor and a novel multilayer inductor. The electromagnetic modelling of the investigative model is also presented.

Key words: inductors, electromagnetic modelling, RFIC, multilayer inductor

Introduction. Traditionally, obtaining high inductance or high Q for RF circuits with on-chip spiral inductors, which also require a large surface area, has been a problem [1]. However, the trend has been to pursue better on-chip inductors because the complete system on a single chip has obvious gains. The search is on for novel on-chip spiral, multilayer, and 3-D inductors with large L, small area,

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low loss, and high Q [2]. This requires modelling the inductance characteristics of such structures accurately and efficiently for automated design.

This paper describes recent work on the numerical modelling of on-chip inductor structures, applied to the comparison of inductor geometries, including the traditional spiral inductor and a novel multilayer inductor. Rather than simply treating the conductors as uniform distributions of current, the higher frequency effects are considered as well, based on the exploration of losses due to skin effect [3], significant in the dimensions we work with: for instance, for an aluminium metal layer conductor at 5 GHz, the skin depth is approximately 1.2 μm , less than half the width of a possible inductor or interconnect segment [4].

Our model and analysis method can be used in the design and optimization of higher-Q, higher-L inductors with smaller real estate. RF design calls for accurate, efficiently obtained values of these parameters and of parasitic impedances for tolerance analysis. A numerical model with fewer assumptions than empirical equations and higher efficiency than full-field solvers would be welcome. So would facile comparisons of different inductor structures.

Modelling of a spiral inductor. The total inductance of a structure is the sum of three different components: the internal self-inductance of the conductor, the external self-inductance generated by a current segment. The internal inductance is part of the frequency-dependent current density distribution within the conductor cross-section. This distribution, found by solving the complex Helmholtz equation, is then integrated and yields frequency-dependent impedance:

$$(1) \quad \nabla^2 \vec{J} = (j\omega\mu\sigma - \omega^2\mu\epsilon)\vec{J},$$

$$(2) \quad Z = \frac{E_0}{\oint_{\text{cond.}} \vec{J} \cdot d\vec{s}} = R(\omega) + \omega L_{\text{int,self}}(\omega),$$

where E_0 is the surface electric field.

At this frequency-dependent impedance gives the frequency-dependent resistive loss [5]. Here, the external self-inductance is found by the magnetic flux, Φ [5]:

$$(3) \quad L_{\text{ext,self}} = \frac{\Phi}{I} = \oint \vec{B} \cdot d\vec{s}.$$

The mutual inductances are calculated by the magnetic vector potential approach; for two current loops i and j [7]:

$$(4) \quad L_{m,ij} = \frac{\mu}{4\pi} \frac{1}{a_i} \frac{\oint_i \int_{a_i} \oint_j \int_{a_j} \frac{J_j da_i da_j}{r_{ij}} d\vec{l}_i \cdot d\vec{l}_j}{\int_{a_j} J_j da_j}.$$

We model the inductance of a spiral inductor as an inductance matrix, L . In the s -domain:

$$(5) \quad \begin{bmatrix} V_1 \\ V_2 \\ \vdots \\ V_N \end{bmatrix} = \begin{bmatrix} L_{11} & L_{m,12} & \cdots & L_{m,1N} \\ L_{m,21} & L_{22} & \cdots & L_{m,2N} \\ \vdots & \vdots & \cdots & \vdots \\ L_{m,N1} & L_{m,N2} & \cdots & L_{NN} \end{bmatrix} \cdot s \begin{bmatrix} I \\ I \\ \vdots \\ I \end{bmatrix}.$$

The mutual inductances of different pairs of spiral segments are shown in Fig. 1. N is the number of spiral turns. The total number of segments is $4N$. A spiral inductor of width $8 \mu\text{m}$ with four turns was used to lay this out, and the edge-to-edge spacing between parallel segments was $2 \mu\text{m}$. The spiral was $11.7 \mu\text{m}$ above the ground plane, and the conductor was assumed to have a thickness of $0.86 \mu\text{m}$. The total length of the inductor was $2000 \mu\text{m}$. Table 1 shows the different parameters of the proposed inductor.

In Eq. (3), Φ is evaluated by integrating the magnetic flux density created by a real current and its image concerning the ground plane. The integration surface bounds are the current segment, the ground plane, and the virtual boundaries, which are perpendicular to the current and the plane.

The shape of the interconnect cross-section can be approximated to be rectangular. The rectangular coordinates are applied as shown in Fig. 2, where z is the direction of the current path.

Equation (1) describes the impedance of a conductor subject to skin effect [5]. The imaginary part of this impedance gives the inductance. In the Helmholtz equation, we considered the geometry of a metal layer in a standard CMOS process, approximately a rectangular cross-section. For a state-of-the-art process, the

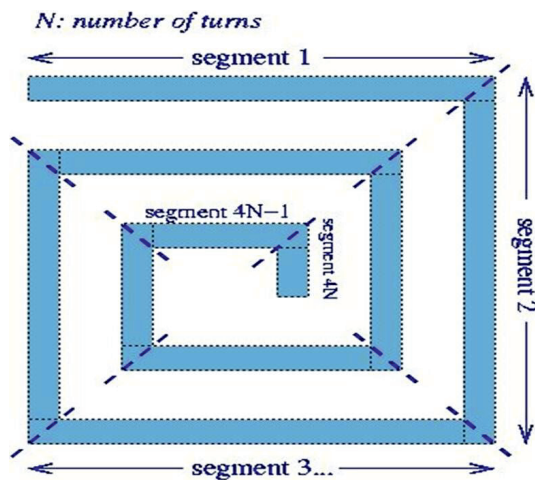


Fig. 1. A spiral inductor with each portion of the turns taken as distinct current segments

Table 1

Parameters for spiral inductor

Parameters	Inductor design
Number of turns (N)	4
Inductor width (W)	$8 \mu\text{m}$
Thickness	$0.86 \mu\text{m}$
Total length(L)	$2000 \mu\text{m}$

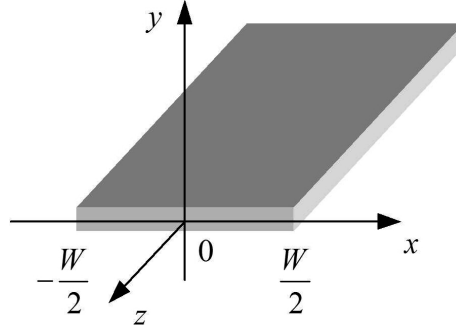


Fig. 2. Skin effect of on-chip interconnects

thickness of the metal layer used to build the spiral inductor would be less than double the skin depth for the frequency of operation [6]. High frequency components suffer more from signal attenuation than the lower frequency components. This is mainly because the skin effect in the substrate becomes more significant at higher frequencies [7]. The Eddy current shields the magnetic field from penetrating further into the substrate. Therefore, the more Eddy current induced near the substrate surface, the more return current flows in the substrate instead of the metal plate. This gives rise to the effective resistance of the interconnect and thus the signal attenuation.

The current distribution on the conductor cross-section is not uniform as long as the current varies with time [8]. This non-uniform distribution is due to the skin effect, which is a frequency dependent phenomenon.

The induced electric field causes a displacement current that in turn adds to the magnetic fields

$$(6) \quad \vec{\nabla} \times \vec{H} = \vec{J} + \frac{\partial \vec{D}}{\partial t}.$$

It is evident that the induced electric field points to the direction that tends to cancel the conducting electric fields at the centre of the conductor and reinforce it at the surface. From Ohm's Law, therefore, the current will crowd at the conductor surface and void at the centre. The skin effect becomes more significant at increased frequencies.

From the carrier transportation point of view, the current density can be written as

$$(7) \quad \vec{J} = qn\vec{v}.$$

For good conductors like metals, the non-uniform distribution of current density as a result of skin effect is mainly due to the non-uniform distribution of the carrier velocity rather than the carrier density. This is because the conductivity

of metals is so high that it is a good approximation that the electron density is uniform throughout the conductor. Thus the skin effect in good conductors can also be viewed as the non-uniform distribution of the electron velocity, which is higher at the conductor surface than the centre [9].

The extreme case will be a superconductive conductor, whose conductivity is infinite. The whole current will flow at the surface of the conductor. There will be only surface current and no body current. Since the carrier density is assumed to be uniform, there will be no normal electric fields perpendicular to the conductor surface, but only tangential ones along the current path [10].

A useful parameter called skin depth is defined to describe quantitatively the skin effect, which is defined as

$$(8) \quad \delta = \frac{\sqrt{2}}{\sqrt{\omega\mu\sigma}}.$$

The skin depth is derived as the depth at which the magnetic field can penetrate a conductor. It is also consistent with the depth beneath the surface of a conductor at which the current mainly flows.

For on-chip interconnects, the thickness of the metal interconnects ranges roughly from 0.5 to 1 μm . The skin depths of different metal layers versus frequency are compared in Fig. 3. It is seen that in the typical radio-frequency range from 1 GHz to 10 GHz, the skin depth varies around several micrometers. Since higher metal layers have better conductivity, they have smaller skin depth than the lower layers. Within our frequency range the skin depth will fall below our substrate thickness around 5 GHz for p-type substrate and around 2 GHz for n-well substrate, lower for active regions [11].

Current crowding effect and the simulation results. For on-chip interconnects, we initially worked on a single current segment, aluminium or copper interconnect piece with 8 μm width. For this size the current distribution within the conductor is mostly uniform up to roughly 1 GHz, so the resistance and internal self-inductance values stay constant. After that point, current crowding at corners gets significant and resistance raises as the effective area of current flow decreases. Simultaneously, the inductance decreases through two mechanisms: Equation (1) demonstrates that for the same complex impedance, the inductance will decrease with increasing ω ; the E-field solutions reveal that the magnitude ratio of imaginary current to real current also decreases as frequency increases, which also will lead to lower L by Eq. (1).

We have also investigated the frequency-dependent coupling between two spiral inductors, which is a result of their mutual inductance. This effect can be troublesome, for instance, in an RF receiver architecture, where the backwards signal leak is unwanted. After the conventional spiral inductor, we have investigated the inductance of a multi-layer inductor in an effort to compare the two structures.

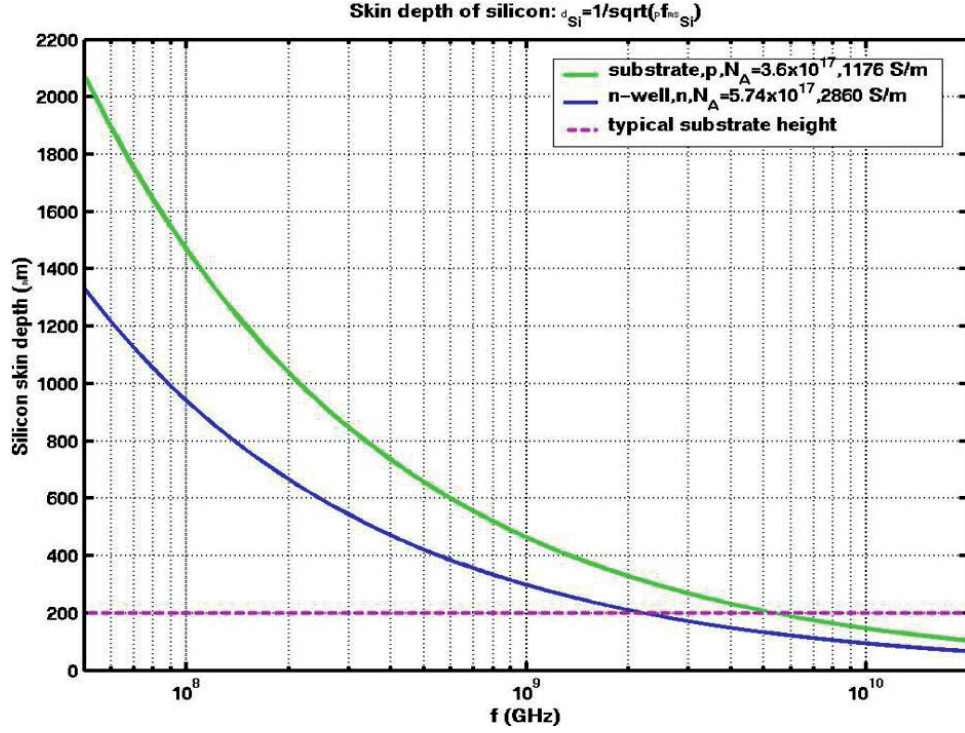


Fig. 3. Comparison of skin depths

After the conventional spiral inductor, we have investigated the inductance of a multi-layer inductor in an effort to compare the two structures. A general multi-layer structure is schematically depicted. We designed this second structure with the same conductor length, 2000 μm . This ensures that both inductors have the same parasitic resistance at the same frequency. This was a four-layer, 2 turns-per-layer inductor with the layers distance from the ground plane 2.7, 4.4, 7, and 11.7 μm , respectively, from bottom to top. We simulated this structure at four frequencies; the results are plotted with the planar spiral results in Fig. 4. We observe that the multilayer inductor yields higher inductance values for these dimensions. Computer simulation gives accurate results compared with the published data simulated by HFSS.

Next, we simulated a spiral inductor with four turns ($N = 4$). The aluminium layer used to lay this out was 8 μm wide, and the edge-to-edge spacing between parallel segments was 2 μm . The spiral was 11.7 μm above the ground plane, and the conductor was assumed to have a thickness of 0.86 μm [12]. The total length of the inductor was 2000 μm . Even though the internal inductance decreases in this frequency domain, the mutual inductance between the segments of the spiral, of a higher order of magnitude than the internal inductance, increases with frequency, and thus the result is a net increase.

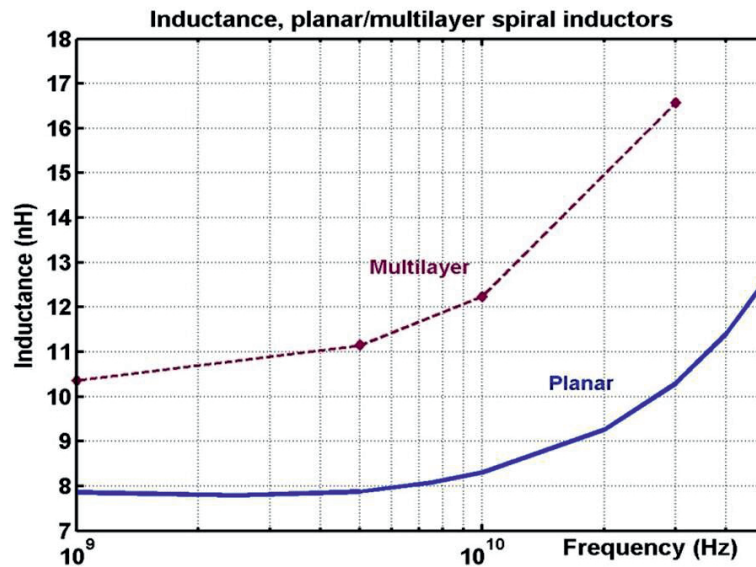


Fig. 4. Comparison of a planar spiral inductor and a multilayer inductor

Discussion. The analyzer was used for this analysis. The noise is -108 dBc/Hz and -128 dBc/Hz at an offset frequency of 100 kHz and 1 MHz, respectively, from the carrier. It may be noted that if differential output was measured, the phase noise will be lowered by 6 dBc since the oscillation amplitude would almost double. The supply voltage is 1.8 V and the VCO core consumes a power of 5 mW. The VCO was tuned with an inversion mode pMOS varactor and it operated from microwave frequency range. The measured phase noise of the VCO is -99 dBc/Hz at 100 KHz and 108 dBc/Hz at 1 MHz offset frequency with power consumption of 5 mW. The VCO was tuned with an inversion mode PMOS varactor and it operated in the microwave frequency range.

Conclusion. In this study, an efficient technique for multilayer on-chip spiral inductors has been developed and tested for any dimension of the spiral inductor by changing the process parameter. This technique can achieve a higher Q-factor. The proposed multilayer on-chip spiral inductor is designed based on the fabrication rules of 180 nm, which is a layout-specific model. The on-chip area of these proposed inductors is very low when compared to planar inductors. A multilayer spiral inductor was implemented.

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