

COMPACT LOW-DROPOUT LINEAR REGULATOR DESIGN
IN 0.13 μm CMOS TECHNOLOGY FOR IoT BASED
REMOTE INFECTIOUS DISEASE MONITORING SYSTEM

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Abstract

With the widespread adoption of the internet of things (IoT), power management of the different electronic (i.e. IoT) devices has become a major challenge. The low-dropout linear regulator (LDO) circuit is widely used for power management applications of electronic devices. This article reports the design and simulation of a low-dropout linear regulator (LDO) circuit, powered by a 1.2 V DC power supply voltage. In order to optimise the power dissipation, low layout silicon area and lower dropout voltage, a current mirror based transistor optimised LDO circuit has been implemented. The simulation results show that the proposed LDO regulator circuit exhibits a 582 mV low-dropout voltage, 1.568 mW power dissipation, and a very compact layout silicon area of $163.84 \mu\text{m}^2$ ($12.795 \times 12.805 \mu\text{m}$). The proposed LDO linear regulator architecture is designed and validated in 0.13 μm TSMC CMOS process technology using Mentor Graphic EDA tools.

Key words: complementary metal oxide semiconductor (CMOS), Internet of Things (IoT), low-dropout regulator (LDO), low power

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Introduction. The critical patients, particularly those who need isolation or quarantine such as COVID-19 infected ones, require continuous remote monitoring of their health parameters to facilitate proper diagnosis and medication. However, existing monitoring stations with wired sensors need attending by the doctors and nurses at regular intervals (if not continuously). Therefore, they are not convenient and/or safe for monitoring the patients infected by contagious diseases. Emerging technologies, such as the internet of things (IoT) and cloud computing, can be integrated to develop a real-time healthcare monitoring system incorporating different ‘varifocal’ wireless sensors. These sensors can transmit the ‘sensed’ data to the linked cloud servers using reliable and high-performance RF communication devices.

The internet of things (IoT) is a system of interconnected computing and communication devices possessing unique identifiers (UIDs) and has the capability of exchanging data without requiring direct human interaction. IoT devices are ‘smart’ enough to spontaneously communicate with each other, whenever there is a necessity for information interchange. The connectivity, networking and communication protocols used with these devices largely depend on the specific IoT applications deployed. As we keep on forwarding, IoT is expected to find its implementation in almost all facets of ‘smart’ human life, where everything will be connected through wireless networks for exchanging real-time information amongst different nodes for accurate and prompt decision making. Today’s, smart health care, smart homes, smart traffic, smart household devices, and smart industries use IoT and relevant other technologies for a better, comfortable and ‘smart’ world. However, due to such profusion incorporation of IoT networks, power management for portable IoT devices has become a concern for the design engineers, particularly with regards to battery run-time. The healthcare monitoring systems, being mission-critical, always need uninterrupted services to provide continuous monitoring, diagnosis and treatment to critical patients. Therefore, it is essential to design and develop an efficient power management system, adhering to such requirements of any healthcare or mission-critical system.

Since the last decade, IoT system development has experienced rapid growth due to the advancement of complementary metal oxide semiconductor (CMOS) technology. In fact, CMOS technology possesses great potentials to meet the inherent stringent cost constraints of the IoT applications [1]. In the radio frequency (RF) regime, the silicon CMOS technology offers multifaceted benefits, due to mainly its economic structure as well as for the potentials it holds with regards to integrating with the silicon MOS-based mixed-signal circuitry. With the recent advancement of CMOS technology, it can now offer cost-effective integration of various technologies and functions, such as RF, digital and analogue functions, on a single chip [2]. As a result, CMOS-based circuits are considered a prospective solution for contemporary IoT devices to satisfy the demands for cost and power-efficient optimised design [3].

Low-dropout linear regulators (LDO) have been widely used in power management integrated system modules and circuits which produce a stable and constant regulated output voltage regardless of the variation in the load [4]. Over the past few years, most of the products operated by mobile or portable battery as well as hand-held electronic devices, such as cell phones, cameras, laptops, PDAs, MP3 players and other multimedia entertainments, have observed extensive market growth and demand, due to efficient and well-organised power management atmosphere. As a matter of fact, over the last decade, both academia and the industry have demonstrated keen research interests in power management ambience [4], resulting in the innovation of various advanced technologies in this domain.

A power management system typically consists of a low-dropout (LDO) linear regulator, switching regulator, control logic and switch capacitor regulator (SCR). It is used in various types of electrical products thus having varied applications, performance and characteristics. Most of the manufactured products, that utilise LDO linear regulator designs, will offer low, stable and constant supply voltage environment while experiencing very subtle differences between the input and the output voltages [4].

However, despite offering all the benefits as discussed above, LDO linear regulators also have some drawbacks in their implementations, for example, transient response, power supply rejection (PSR), narrow-loop bandwidth, large on-chip capacitor, high power consumption, etc. Therefore, LDO linear regulator design needs to incorporate several features for better performance trade-off, as explained in [5–12].

In this article, an optimised design of the LDO linear regulator has been proposed using Mentor Graphic EDA tools adopting 0.13 μm TSMC CMOS process technology. The proposed design was implemented with slight modification through the provision of adjustable external components. For the performance evaluation of the proposed LDO regulator circuit, the parameters such as power dissipation, layout silicon area and dropout/supply voltage condition were considered. The proposed LDO is likely to contribute to the widespread adoption of IoT devices equipped with better power management systems.

LDO design strategy. The overall design of the proposed LDO linear regulator circuit consists of an error amplifier, a series pass element (PMOS Pass Transistor), a sampling resistor network, an off-chip external capacitor, voltage reference (V_{ref}), input voltage and load, shown in Fig. 1.

An error amplifier (M1-M8, P2-P3), as shown in Fig. 1, is used to compare the different variations between the feedback voltage and the reference voltage, by producing an error signal. It also adjusts the gate voltage of the PMOS pass transistor to control the current accordingly, in order to meet the requirement of the output voltage. As to maintain the constant output voltage at the load, the output from the error amplifier acts directly as a controlling input for the PMOS

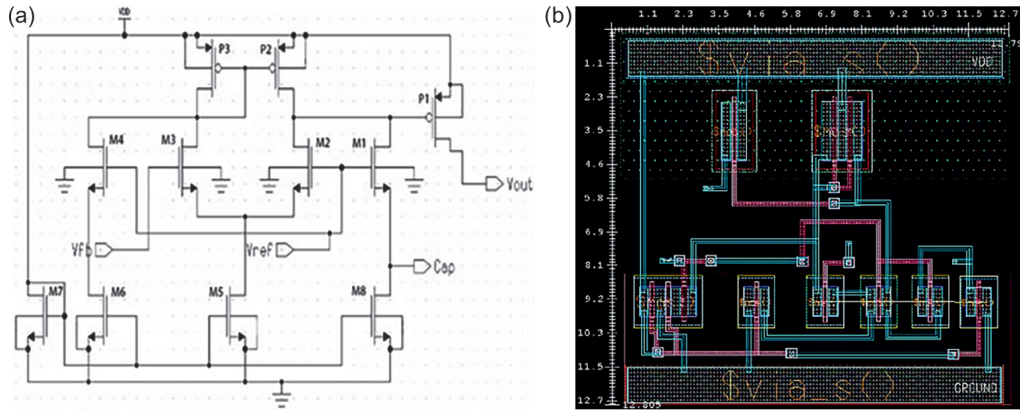


Fig. 1. (a) Schematic and (b) layout diagram of the proposed LDO linear regulator, without resistor network and capacitor

pass transistor, to supply variable current. An operational amplifier is used as a two-stage error amplifier to obtain the robustness of the performance parameter and to overcome the instability.

PMOS pass transistor (P1) has a higher output impedance. Therefore, it is used to deliver a high current from the source voltage, as required by the load, to maintain the constant output value. PMOS pass transistor is also controlled by its gate voltage since it is smaller than the source voltage. The aspect ratio of the PMOS pass transistor is typically large so that it can deliver the maximum load current and generate low-dropout voltage for a given application.

A sampling resistor network is used to generate feedback voltage (V_{fb}) from the output voltage to a suitable value by comparing it to a reference voltage and then passing it to the input of the error amplifier. A proper voltage reference (V_{ref}) is generally employed and is used in the regulator design in order to meet the requirements for achieving high accuracy as well as low output voltage. In this design, the value of the reference voltage is set to 1.22 V. The off-chip external output capacitor is used to provide the stability that makes use of its equivalent series resistance (ESR) and improves the transient response.

In this design, the appropriate aspect ratio of the PMOS and NMOS transistors (P1-P3, M1-M8) were chosen using the trial and error method. From our research results, it is evident that the optimisation of power dissipation has been achieved. Although the dynamic power dissipation has been trimmed down by minimising the gate, using the transistor sizing technique, which in turn reduces both the length and the width of the transistors. As a result, the LDO linear regulator remarkably minimises the power dissipation.

In this study, the LDO linear regulator design has been augmented through optimised transistor sizing for error amplifier and current mirror. The aspect ratio of the PMOS transistors (P1, P2 and P3) is set to $W/L = 2 \mu\text{m}/0.13 \mu\text{m}$

and for NMOS transistors (M1, M2, M3, M4, M5, M6, M7 and M8) is set to $W/L = 1 \mu\text{m}/0.13 \mu\text{m}$, for the proposed LDO linear regulator.

In order to achieve the ideal current matching, improved output resistance and high input impedance characteristics over a wide range of swing of voltages, a current mirror technique is applied to the LDO linear regulator design [7]. It is designed to copy a current through one active device by controlling the current in another active device of a circuit, while keeping the output current constant. This technique focuses on the error amplifier circuits in the internal elements. The output current at the two-terminal circuit (P2 and P3) depends only on the input current and is independent of the output terminal voltage, regardless of the load.

Our research reveals that the LDO linear regulator design consumes very low power and low layout silicon area. These results are likely to be due to the application of optimised transistor sizing and current mirror with both PMOS and NMOS transistors. Moreover, the occupied core silicon area of the proposed LDO layout is $(12.795 \times 12.805) \mu\text{m}^2$, as shown in Fig. 1.

Results and discussion. The proposed LDO linear regulator has been designed and verified using Mentor Graphic EDA Tools using $0.13 \mu\text{m}$ TSMC CMOS process technology with $V_{DD} = 1.2 \text{ V}$, $V_{\text{ref}} = 1.22 \text{ V}$. In this research, the performance of the LDO regulator circuit is assessed by the simulation results at a standard temperature of 300 K .

To determine the proposed LDO linear regulator's output voltage, the transient and AC analysis was performed. The transient output voltage obtained for the LDO is 0.618 V , as shown in Fig. 2(a). The simulation result of the loop gain, as well as the phase response of the proposed LDO linear regulator, is shown in Fig. 2(b). It demonstrates that a 55 dB gain is achieved for a bandwidth of approximately 10^5 Hz .

In order to locate the best low-dropout voltage of the proposed LDO linear regulator, a simulation was carried out at different regulating input voltages, ranging from 0 V to 3.5 V whereas other parameters remain unchanged, as shown in

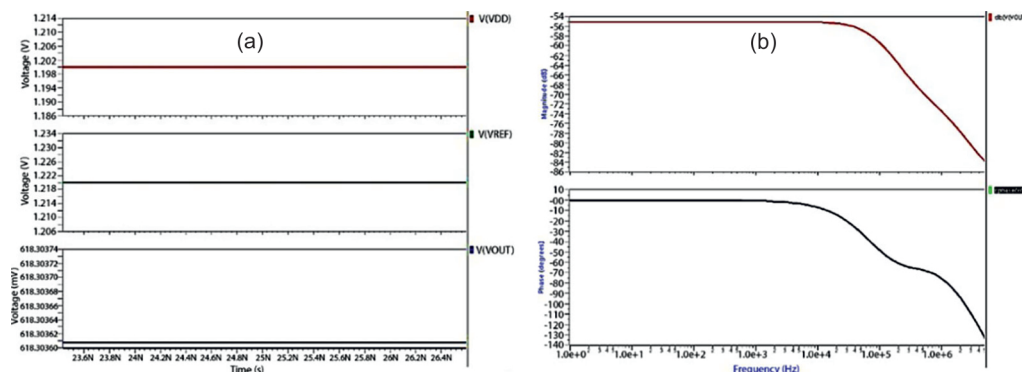


Fig. 2. (a) Transient and (b) AC analysis of the proposed LDO linear regulator

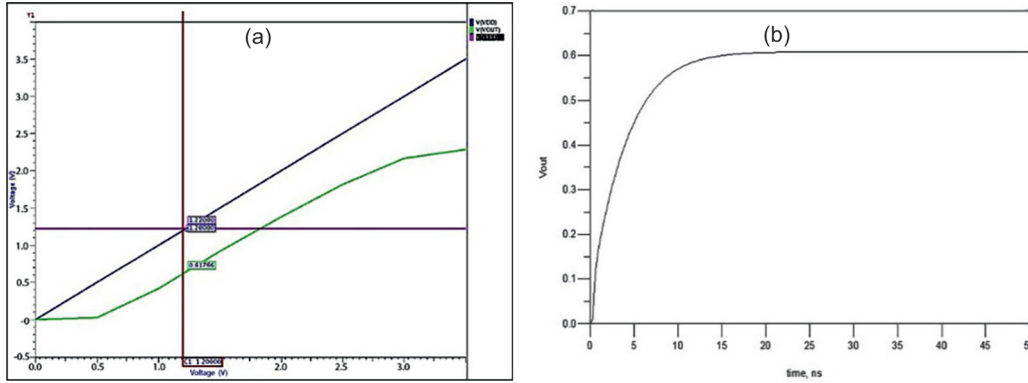


Fig. 3. (a) Parametric sweep simulation of input voltage vs. output voltage and (b) step response of the proposed LDO linear regulator

Fig. 3(a). From the simulation, it is clearly evident that by regulating the input voltage, the achieved dropout voltage remains remarkably small. The area, under the graph in-between $V(VDD)$ and $V(OUT)$, represents the low-dropout voltage of the LDO. This supports the fundamental aim of designing the regulator, i.e. to achieve a long battery life. In order to ensure the best low-dropout voltage, the input voltage is set to 1.2 V that exhibits a dropout voltage of 582 mV. Moreover, the LDO output is getting stabilised approximately after 15 ns time as evident from the step response simulation at 1.2 V input voltage condition as illustrated in Fig. 3(b). The LDO dissipates only 1.568 mW power for its functioning, from a 1.2 V DC power supply.

A performance comparison summary of various technologies amongst state-of-the-art LDOs is listed in Table 1. Compared to other researches, it is observed that the proposed LDO linear regulator design acquires the lowest layout silicon area of only $163.84 \mu m^2$. This is mainly due to the adoption of optimised small-size transistors as well as avoidance of bulky passive constituents like capacitors, re-

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Summary of the LDO performance comparison

Reference	CMOS Technology	Input Voltage (V)	Output Voltage (V)	Dropout Voltage (mV)	Power (mW)/ Max current (mA)	Chip Size (mm^2)
[7] 2016	0.18	1.4	1.2	200	50 mA	0.039
[12] 2017	0.25		3.3	230	100 mA	0.21
[11] 2018	0.065	0.6	0.5	100	45 mA	0.045
[10] 2020	0.18	1.3	1.09	0.21	11 mA	0.105
[9] 2020	0.18	1.5–2	1.5	19.3	50 mA	2.96
[8] 2020	0.5	1.5–5	4.8	200	100 mA	0.082
This work	0.13	1.2	0.618	582	1.568 mW	$163.84 (\mu m^2)$

sistors, etc. Moreover, the LDO exhibits a very competitive result of low-dropout voltage of 582 mV and low power dissipation of 1.568 mW, which can be operated at a reasonably low supply voltage condition of 1.2 V. It also indicates that the proposed LDO is not limited by the process technology or the types of the applications.

Conclusion. In this paper, an LDO linear regulator has been proposed for the power management application of modern IoT devices. The design exhibits a very compact core layout area of 163.84 μm^2 . Simulation results show that the designed LDO linear regulator can provide a low-dropout voltage of 582 mV. Moreover, the proposed LDO linear regulator is appropriate for optimising the power dissipation and is suitable to operate at lower supply voltage conditions. The proposed LDO linear regulator design has the superiority to adjust or change the internal and external elements accordingly. Therefore, it can be concluded that such fully integrated LDO regulator will significantly contribute to meeting the demands of the low-power compact IoT devices for remote infectious disease monitoring station applications.

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